Microelectronics and Solid State Electronics 2014, 3(1A): 1-8
DOI: 10.5923/s.msse.201401.01

Guideline on Quantitatively Analyzing Analog Nano-Scale CMOS Circuits Using Ultra-Compact Model

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Abstract This paper presents a tutorial about analyzing analog nano-scale CMOS circuits quantitatively. A ultra-compact model which is numerically accurate is essential in the analysis. Besides, the characteristics of nano-scale MOSFET must be considered. The nonlinear output conductance and the cross-terms among the controlling voltage cannot be ignored in nano-scale circuits. Distortion analysis of nano-scale gate-driven and bulk-driven amplifier is performed as a demonstration of this guideline.

Keywords CMOS, Bulk-driven, Distortion, Model

1. Introduction

Owing to the reducing channel length of metal – oxide – semiconductor field-effect transistor (MOSFET), the performance of complementary metal-oxide-semiconductor (CMOS) integrated circuits (IC) has been improved greatly, such as power consumption, speed and noise [1-3]. Meanwhile, bulk-driven (BD) technique has been proposed to tackle the harsh voltage-swing challenge in modern low voltage design [4]. BD MOSFET works in a depletion mode which allows negative, zero and small positive bias voltage at the bulk terminal. This technique increases the input common mode range as well as the signal swing, which cannot be realized by gate-driven (GD) technique at low V_{DD} [4].

To design high performance nano-scale GD/BD circuits, quantitative analysis is necessary. In order to analyze nano-scale circuits quantitatively, firstly, a current model which characterizes transistor accurately is demanded. Especially for BD circuits, the model must be also accurate when the signal is applied at the bulk-terminal.

To describe the characteristics of nanometer MOSFET, several physic effects have to be included into model, such as the short-channel (SCE) and the narrow width effect (NWE), the mobility degradation (MD), the velocity saturation (VS), the channel-length modulation (CLM), the drain-induced barrier lowering (DIBL) and the source-drain parasitic resistance (S/D-PR) [5]. Berkeley short-channel insulated-gate model (BSIM) [6] provides the highest accuracy; however, it has a large number of parameters and is the most complex model which is simulation-oriented, not suitable for circuit analysis. Comparing with simulation-oriented model, ultra-compact model is more ideal to be applied to analyze circuit [5].

Models can be also selected according to the type of analysis, i.e. qualitative or quantitative analysis. For qualitative analysis, simple model can be used as long as it shows the characteristics of MOSFET in the targeting operational region qualitatively accurately. For example, the model from [7] that covers the subthreshold and moderate inversion regions was successfully applied to analyze the mixing mechanism of BD mixer and new application of BD mixer has been found based on the analysis [8].

For quantitative analysis, such as the numerical calculation of distortion of nanometer GD/BD circuits, ultra-compact model which is numerically accurate for nano-scale MOSFET must be chosen. Reference [5] provides such a model which has ten parameters and is accurate for nanometer MOSFET; however, it was originally proposed to digital applications, not optimized for bulk-driven applications. In this work, the model is modified to be adapted to the characteristics of nano-scale BD transistor. Hence it can be applied to quantitatively analyze BD circuits.

Besides the model selection/adaption, the characteristic of nano-scale MOSFET must be also considered in the analysis. In this research, it is found that the nonlinear output conductance and the cross-terms play important roles in the analysis, although they are often ignored in the analysis of mirco-scale CMOS circuits.

The paper is organized as following. In Section 2, the original model is introduced and modified for BD applications. The results of parameter extraction and fitting are illustrated. The parameters of the model are fitted well with the simulation data which is the premise of the analysis.

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Published online at http://journal.sapub.org/msse

Section 3 shows the importance of the inclusion of the nonlinear output conductance and the cross-terms. The distortion analysis of GD/BD RF amplifier is demonstrated as an example of this guideline. Finally there is a brief conclusion in Section 4.

2. Accurate Current Model for Nano-Scale MOSFET and Its Modification for BD Applications

2.1. Original Current Model

By combining the merits of the previous ultra-compact models [9-12], and by including DIBL, NWE, and S/D-PR, a 10-parameter model was proposed for nano-scale CMOS transistor in [5]:

$$i_{ds} = \frac{i_{D0}}{1+\frac{R_{DS0}\cdot i_{D0}}{\varpi\cdot v_{DS}}} \quad (1)$$

where

$$i_{D0} = \varpi C_I (v_{GS} - V_{th})^n [1 + \lambda(v_{DS} - V_{DSAT})], \quad (2)$$

$$V_{DSAT} = C_V (v_{GS} - V_{th})^a, \quad (3)$$

$$V_{th} = V_{th0} + \frac{\eta_{NWE}}{\varpi} - \eta_{DIBL} v_{DS} + \eta_{BB} v_{SB}. \quad (4)$$

C_I and C_V are used to linearly proportionally scale current and saturation voltage; n and a are used to describe the fractional power dependence of the current and the saturation voltage on the overdrive voltage $(v_{GS} - V_{th})$; body biasing (BB), DIBL, and NWE are described by adding corrective terms η_{BB}, η_{DIBL} and η_{NWE} into V_{th}; the transistor width is referred as is the multiple, ϖ, of the minimal allowed width; R_{DS0} is used to describe the impact of S/D-PR; λ is the coefficient of CLM.

This model describes the I-V characteristics accurately in superthreshold region [5]. However, it was originally proposed to digital applications, not optimized for BD applications. In order to perform the quantitative analysis of BD circuits, it is modified in this work to adapt to BD MOSFET and the parameters are fitted to a commercial 65 nm technology used in this research.

2.2. Modified Model for BD Applications

To investigate if the model can describe the characteristics of nano-scale MOSFET accurately, *I-V* characteristic needs to be examined. Furthermore, up-to-three order of derivatives K_{lmn} of i_{ds} over bias voltages have to be fitted. K_{lmn} is defined as:

$$K_{lmn} = \begin{cases} \frac{1}{l!}\frac{1}{m!}\frac{1}{n!}\frac{\partial^{(l+m+n)} i_{ds}}{\partial v_{gs}^l \partial v_{sb}^m \partial v_{ds}^n}\Big|_{\substack{v_{gs}=V_{GS}\\ v_{sb}=-V_{BS}\\ v_{ds}=V_{DS}}} & \text{when } l \neq 0 \text{ or } n \neq 0 \\ (-1)\cdot\frac{1}{m!}\frac{\partial^m i_{ds}}{\partial v_{sb}^m}\Big|_{v_{sb}=-V_{BS}} & \text{when } l = n = 0 \end{cases} \quad (5)$$

$(l+m+n) \in \{1,2,3\}$, and $l, m, n \in N$.

Obviously, $K_{100} = g_m$ $K_{010} = g_{mb}$, and $K_{001} = g_o$, which are the first-order coefficients of the nonlinear (bulk-) transconductance and the nonlinear output conductance, respectively. (K_{200}, K_{300}), (K_{020}, K_{030}), and (K_{002}, K_{003}) are second- and third-order nonlinear coefficient only related to v_{gs}, v_{sb}, and v_{ds}, respectively. Others are the coefficients of the cross-terms among v_{gs}, v_{sb}, and v_{ds}.

In strong inversion region, C_I, n, C_V and a are the most effective parameters to adjust I_D and (K_{100}, K_{200} and K_{300}) versus V_{GS}. Figure 2 shows the results of parameter fitting. Figure 2 (a) shows the drain current I_D versus V_{GS} when $V_{DS} = 0.5$ V. Figure 2 (b) shows K_{100}, K_{200} and K_{300} versus V_{GS} when $V_{DS} = 1$ V and $V_{BS} = 0$ V. The simulation data are obtained from a transistor of $W/L = 60\mu m/80nm$, using BSIM 4 model; The simulation test bench is shown in Figure 1.

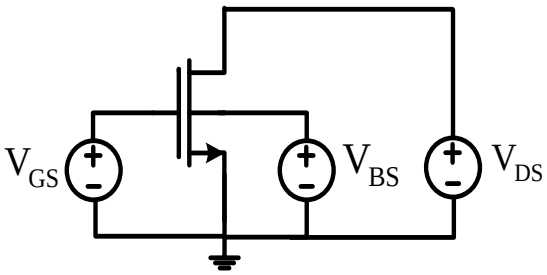

Figure 1. Simulation test bench

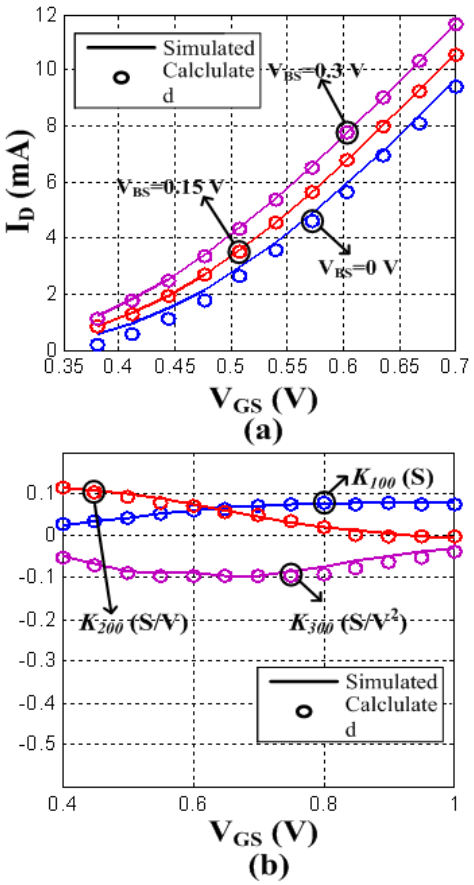

Figure 2. Comparison between the simulated and calculated I_D and (K_{100}, K_{200} and K_{300}) versus V_{GS}

I_D and (K_{001}, K_{002} and K_{003}) versus V_{DS} are mainly controlled by the parameters of λ, η_{DIBL}, C_V and a in

saturation region. Figure 3 demonstrates the comparison of I_D and (K_{001}, K_{002} and K_{003}) versus V_{DS}. In Figure 3 (a), $V_{BS} = 0$ V. In Figure 3 (b) $V_{GS} = 0.5$ V and $V_{BS} = 0$ V. From Figure 2 and Figure 3 show that good fitting of i_{ds} and its derivatives over V_{GS} and V_{DS} are achieved.

In the original model, I_D and (K_{010}, K_{020} and K_{030}) are basically adjusted by n and η_{DIBL}. It is found for the original model in [5] that even if the calculated K_{020} and K_{030} are close to the simulated values, I_D and K_{010} are still underestimated. And if I_D and K_{010} are adjusted to be close to the simulated ones, K_{020} and K_{030} are apart from the simulated values. It is proposed that $-\eta_{BB}' v_{SB}$ is added to the current model to adjust I_D and K_{010} without affecting K_{020} and K_{030}:

$$i_{ds} = f(v_{gs}, v_{sb}, v_{ds})\big|_{originalin\ [12]} - \eta_{BB}' v_{sb}. \quad (5)$$

Figure 4 illustrates the result of the parameter-fitting by comparing I_D and (K_{010}, K_{020} and K_{030}) versus V_{BS}. In Figure 4 (a), $V_{DS} = 0.5$ V. In Figure 2 (b), $V_{DS} = 0.4$ V and $V_{GS} = 0.5$ V. It is clear that without this added parameter, I_D and K_{010} are underestimated. This added parameter gives us one more degree of freedom to achieve accurate fitting of both linear and nonlinear terms.

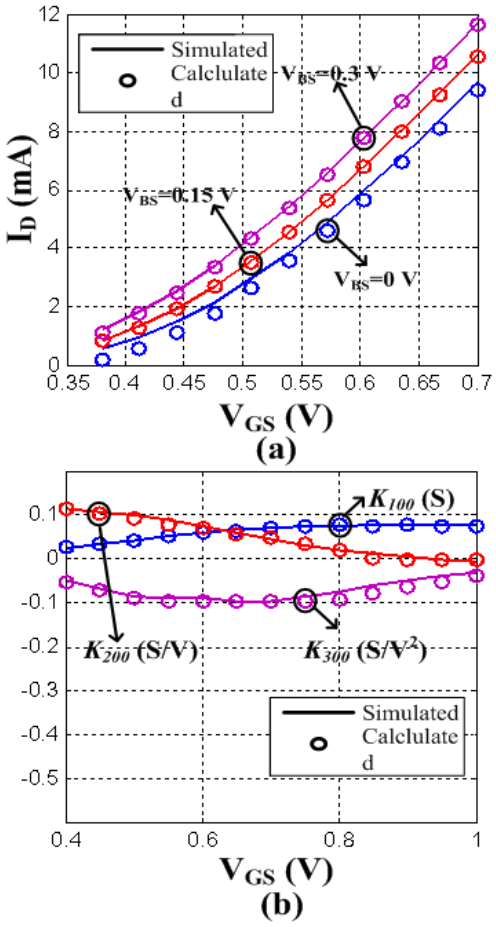

Figure 3. Comparison between the simulated and calculated I_D and (K_{100}, K_{200} and K_{300}) versus V_{GS}

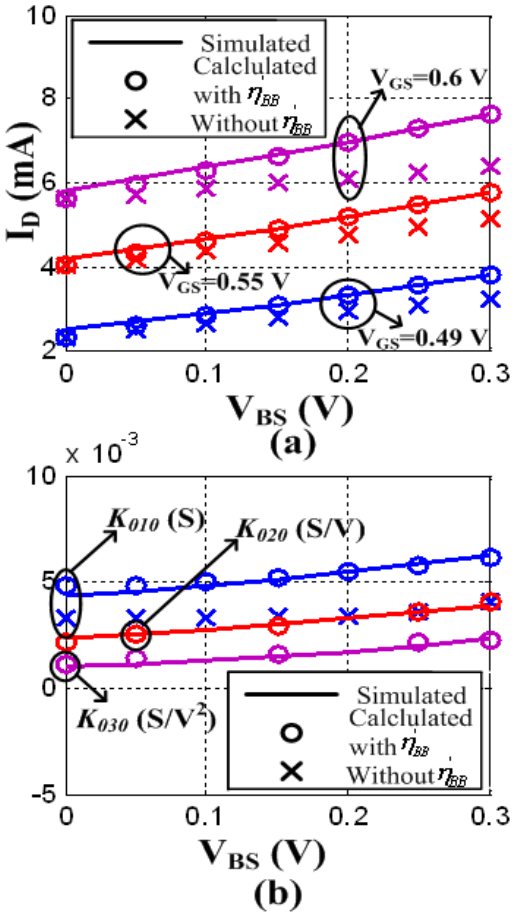

Figure 4. Comparison between the simulated and calculated I_D and (K_{010}, K_{020} and K_{030}) versus V_{BS}

Although in the range of $V_{BS} = 0$ to 0.1 V, I_D is still underestimated (as shown in Figure 2 (a), Figure 3 (a), and Figure 4 (a)) and K_{010} is a little overestimated (as shown in Figure 4 (4)), the fitting parameters can give us reasonable accuracy in quantitative analyses. A current model which is fitted to the used technology accurately is the prerequisite of numerically analyzing nano-scale CMOS circuits.

3. Quantitative Analysis of Nano-Scale Circuits

In Section 2, the model proposed in [5] has been modified for BD transistor; and its parameters have been fitted well. Hence it can be applied to analyze nano-scale CMOS circuits quantitatively, e.g. the distortion analysis of GD and BD amplifier (see Figure 5). The goal of quantitative distortion analysis is to achieve mathematical expressions of the distortions which can predict the nonlinear behavior of the GD/BD amplifier. Using the modified current model in which the parameters are extracted and fitted to the CMOS technology, the bias voltages can be applied as inputs of the expressions of

distortions, and the distortions can be acquired as the outputs [13-15].

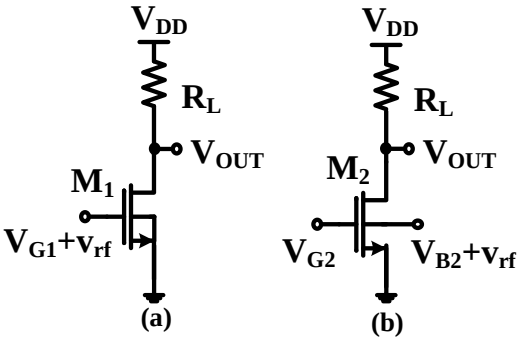

Figure 5. Schematic of GD amplifier (a), and BD amplifier (b)

It is imperative to acknowledge that the output conductance and the cross-terms among the controlling voltages must be included in the quantitative analysis of nano-scale CMOS circuits, although for the distortion analysis of GD CMOS circuits in micrometer scale, their effects were often ignored [13, 16, 17]. It is found that this exclusion would cause serious distortion calculation error in the analysis of deca-nano scale CMOS circuits and the failure to predict the effect of the increasing of the overdrive voltage and the source degeneration resistance, even if this accurate model is used in the analytical calculation. This can be demonstrated in Figure 6 to Figure 9, showing the value of harmonic distortion (HD) of GD and BD RF amplifier in a 65 nm technology, respectively. The GD/BD amplifier is shown in Figure 5, both of which have the size of $W/L = 60\ \mu m/80\ nm$, $R_L = 400\ \Omega$ and $v_{rf} = 1\ mV@2\ GHz$. The the expression of HD_2 and HD_3 of the GD and BD amplifier can be found in [14, 15], respectively.

From Figure 6, it is clear that there is significant error between the simulated and the calculated second-order and third-order harmonic distortion (HD_2 and HD_3) if only the nonlinearity of the transconductance is considered in the analytical calculation. The calculation cannot even predict the trend of behavior of HD. It is also found that the effect of the source degeneration resistance (R_S) depends on the bias point in this study. Under certain bias condition, the increase of R_S cannot reduce HD monotonically, as shown in Figure 7, where the bias current is 3.2 mA. However, if the contribution from the nonlinear output conductance and the cross-terms is excluded, the nonlinear term only from the transconductance is reducing continuously with R_S, i.e. the value of $\frac{K_{200}}{g_m(1+g_m R_S)^2}\ (V^{-1})$ and $\frac{K_{300}}{g_m(1+g_m R_S)} - \frac{2K_{200}^2 R_S}{g_m(1+g_m R_S)^4}\ (V^{-2})$.

Similar finding is made in nano-scale BD amplifier as shown in Figure 8 and Figure 9. Figure 8 shows substantial error exits if the nonlinearity of the output conductance and the cross-terms are excluded. In Figure 9 (a), taking only the nonlinearity from the body-transconductance into consideration will overestimate the effect of R_S on HD_2. Nearly 20 dB reduction of $HD_2 = \frac{1}{2}V_{in}\left|\frac{K_{020}G_S^2}{(G_S+g_{mb})^2 g_{mb}}\right|$ is expected if only the nonlinearity from the body-transconductance is considered; however, only about 6 dB reduction is obtained by simulation. For HD_3, simulation shows that at this bias condition (the bias current is 2.5 mA), R_S cannot be used to reduce HD_3; however, calculation of the term that only includes the nonlinearity of the body - transconductance, i.e. $\frac{K_{030}(G_S+g_{mb})G_S^3 - 2K_{020}^2 G_S^3}{(G_S+g_{mb})^4}\ (V^{-2})$ shows an opposite change of HD_3 with R_S, as shown in Figure 9 (b). Here, $G_S = (R_S)^{-1}$.

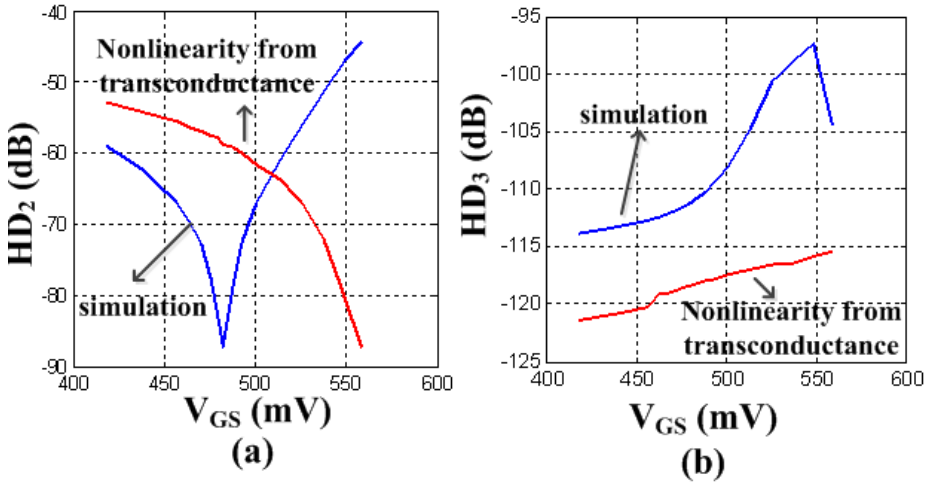

Figure 6. Comparison of the simulated HD_2 (a) and HD_3 (b) versus V_{GS} of the nano-scale GD amplifier with the calculated HD which only includes the nonlinearity of the transconductance

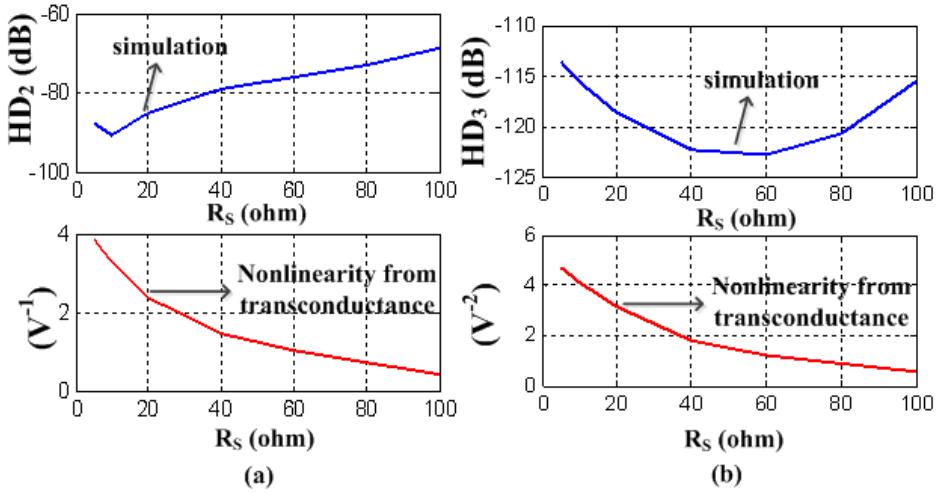

Figure 7. Comparison of the simulated HD_2 (a) and HD_3 (b) versus the source degeneration resistance of a nano-scale GD amplifier with the calculated HD which only includes the nonlinearity of the transconductance

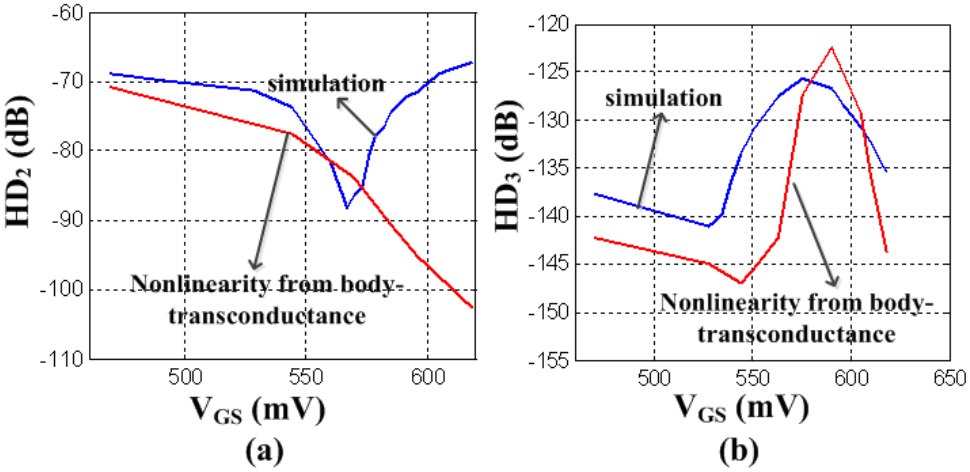

Figure 8. Comparison of the simulated HD_2 (a) and HD_3 (b) versus V_{GS} of thenano-scale GD amplifier with the calculated HD which only includes the nonlinearity of the transconductance

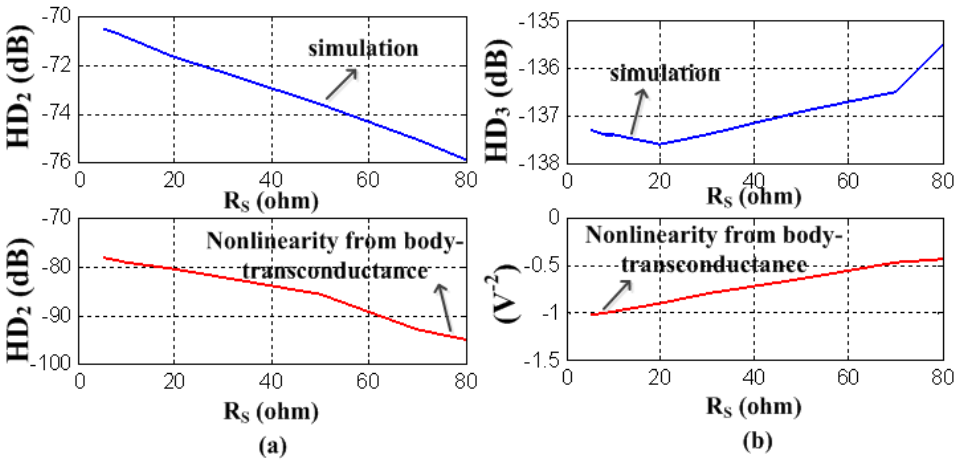

Figure 9. Comparison of the simulated HD_2 (a) and HD_3 (b) versus the source degeneration resistance of a nano-scale GD amplifier with the calculated HD which only includes the nonlinearity of the transconductance

Therefore, for nano-scale CMOS circuit, the effect of the nonlinear output conductance and the cross-terms must be included; otherwise the distortion analysis is far from being accurate, based on which the linearization techniques are not practical.

On contrast, by including the output conductance and the cross-terms, using this modified ultra-compact model, calculation gives good agreement with the simulation result.Moreover, the distortion behavior can beinterpreted quantitatively owing to the accurate ultra-compact model. Next, HD_3 of the GD amplifier and HD_2 of the BD amplifier are analyzed as demonstrations [14, 15].

Figure 10 (a) and Figure 11 (a) shows that by using the modified model, the analytical calculation which includes the effects of the output conductance and the cross-terms provides satisfactory accuracy, comparing with the simulation. Furthermore, by analyzing the dominant terms in the HD_3expression, the trend of HD_3 can be interpreted in Figure 10 (b). It is found that $|K_{300}/g_m|$ increases continuously. Besides, when $V_{GS} > 480\ mV$, $|A_v^2(K_{120}/g_m)|$, $|A_v^3(K_{003}/g_m)|$, and $|3A_v^2(K_{002}K_{110}/g_m)(1/g_o + G_L)|$ increase substantially and become the major parts of HD_3; also, the last one has opposite sign against the first two, thus the total of them, i.e. HD_3, shows the characteristic shown in Figure 10. Here, $A_v = g_m/(g_o + G_L)$, g_o is the output conductance and G_L is the load. From Figure 11 (b), it is realized that although the amplitude of the K_{300}- and K_{200}-related term is monotonically reduced by R_S, the amplitude of the K_{210}-, K_{120}-, and K_{003}- related terms is parabola, especially the K_{120}-related term becomes the major part when $R_S > 60\ \Omega$. Thus, the total of all the terms in HD_3 behaves as parabola and starts increasing when $R_S > 60\ \Omega$.

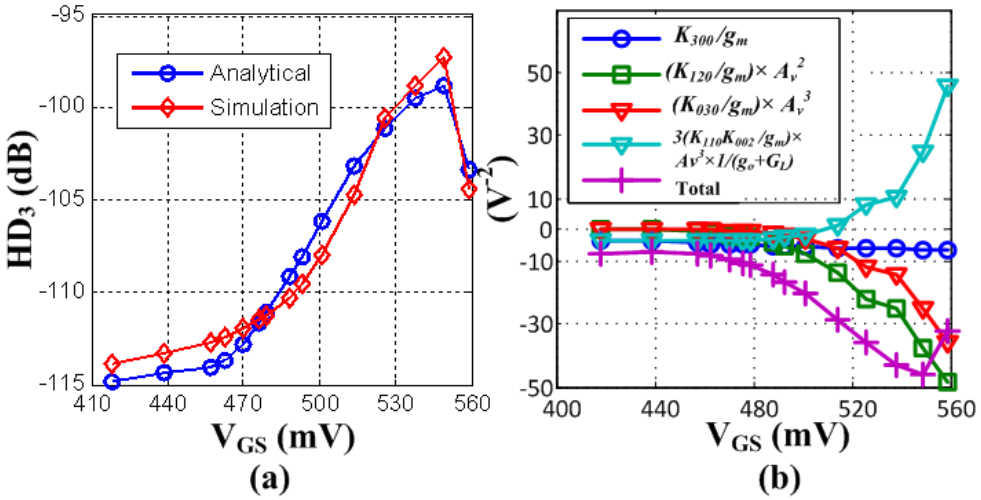

Figure 10. (a) Analytical and simulated HD_3, and (b) K_{030}/g_{mb}, three other major contributions, and the sum of all the terms in HD_3

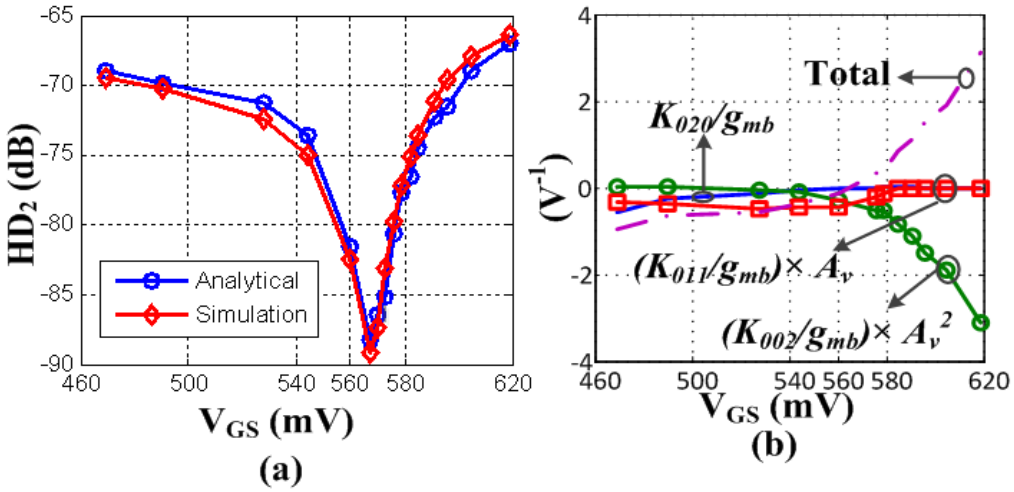

Figure 11. Effect of R_S: (a) the analytical and simulated HD_3; (b) the contribution of the dominantterms to HD_3 under 3.2mA bias current

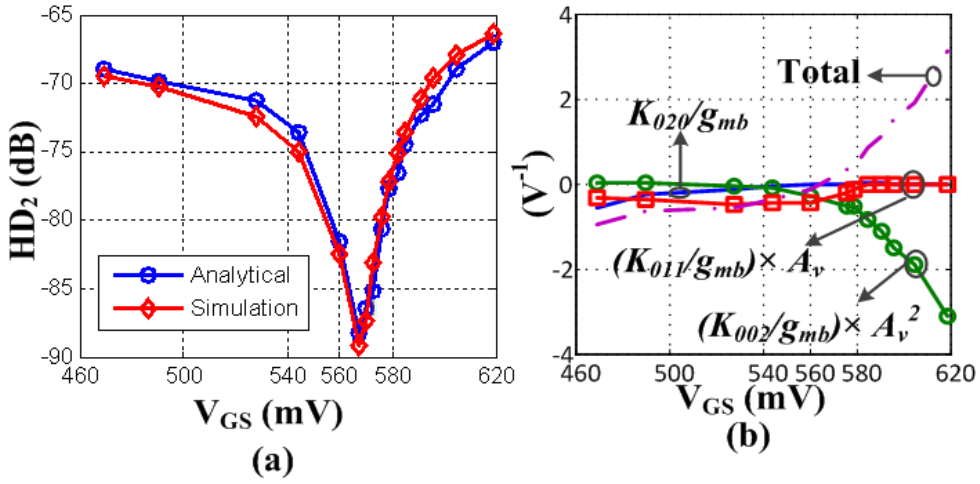

Figure 12. (a) Analytical and simulated HD_2 when $V_{BS} = 0$ V, and (b) the contribution of each term and the sum of all the terms in HD_2

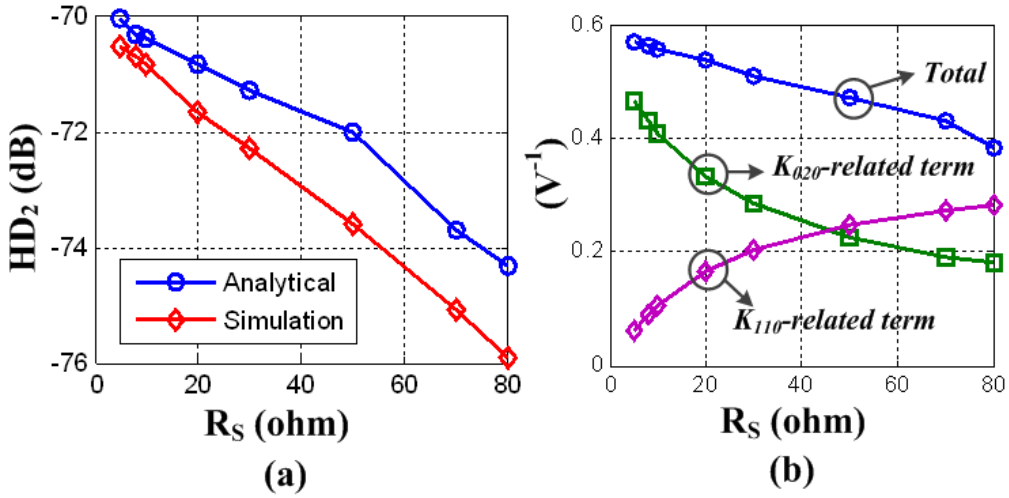

Figure 13. K_{020} and K_{110}-related terms in HD_2 and the total of all the terms in HD_2 versus R_S under 2.5mA bias current and $V_{BS} = 0$ V

Similarly, for the BD amplifier, after taking into account the output conductance and the cross-terms, good accuracy is achieved in the calculation using this model, as shown in Figure 12 (a) and Figure 13 (a). Figure 12 (b) explains the behavior of HD_2 of the BD amplifier: K_{020}/g_{mb} contributes less as V_{GS} increases; however, $-A_v^2(K_{002}/g_{mb})$ increases significantly when $V_{GS} \geq 560$ mV, thus HD_2 is increased. Moreover, the contribution of $-A_v^2(K_{002}/g_{mb})$ cancels that of $A_v(K_{011}/g_{mb})$ since they have the same sign and subtract each other. The values of the two terms are equal around $V_{GS} = 566$ mV, hence there is an optimal region of HD_2. Figure 13 (b) demonstrates the contribution of K_{020} and K_{110} -related terms in HD_2. Although K_{020} contributes less as well known in long channel technology, the contribution of K_{110}-related term increase significantly and counteract against the reduction of K_{020}-related term. Thus HD_2 reduces slower as R_S increases.

By following this guideline, i.e. using an quantitatively accurate model and including the nonlinear output conductance and the cross-terms, HD_2 of the GD amplifier and HD_3 of the BD amplifier can be calculated correctly and each term in the expressions of HD_2/HD_3 can be analyzed to interpret the characteristic.

4. Conclusions

The guideline of quantitatively analysing nano-scale CMOS circuits can be summarized as:

First, anultra-compact model which is numerically accurate for nano-scale MOSFET is required. The parameters in the model have to be fitted the used technology. One of these kinds of models is introduced in this paper, which is modified here to be adapted to BD applications by introducing one new parameter to achieve accurate fitting of both linear and nonlinear terms. This modified model can be applied for analysing nano-scale GD/BD circuits.

Second, for nano-scale CMOS circuits, the nonlinear output conductance and the cross-terms among the controlling voltages, i.e. v_{gs}, v_{sb}, and v_{ds}, must be included; otherwise there would be significant error between the calculated and simulated results.

In this paper, the distortion analysis of nano-scale GD and

BD amplifier is demonstrated as an example to show the importance of the nonlinear output conductance and the cross-terms, as well as the effectiveness of the accurate ultra-compact model.

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