

Simulator of Reactor Kinetics

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Abstract This paper describes the design concepts of digital-to-analog simulators of nuclear reactor reactivity and gives information pattern about power signal which corresponds to fixed value of reactivity. The main design concept for digital-to-analog simulator is decadic partition of power signal level with normalization of decades to the specified number which corresponds to number of bits of digital-to-analog converter (DAC) and storing of the duplicated information concerning the power signal. This paper proposes the design of simulator based on 12-bit DAC. The simulator has $\leq 1\%$ relative error for reactivity value corresponding to output signal of DAC-simulator within three decades of power signal variation.

Keywords Nuclear Reactor, Power Signal, Reactivity, Digital-to-Analog Simulator

1. Introduction

For reactor monitoring, special-purpose calculation instruments called reactivity meters are widely used [1, 2]. Functional principle of reactivity meter is based on the solution of reversed equation of reactor kinetics with input signal proportional to neutron flux [1].

Periodic calibrations and function tests of the reactivity meters should be performed in order to support reliable operation of reactor control system. For this purpose specialized instruments, simulators of reactor kinetics, are used. These simulators can also be used for adjustment of reactivity meters in factory and for testing of instruments of the reactor control and safety system.

The simulator output signal models variation of neutron flux (reactor power) at constant value of reactivity, the variation corresponding to solution of the known set of neutron kinetics equation [3]:

$$\begin{cases} \frac{dn}{dt} = \frac{\rho - \beta}{\ell^*} n + \sum_{i=1}^6 \lambda_i \bar{C}_i, \\ \frac{d\bar{C}_i}{dt} = \frac{\beta_i n}{\ell^*} - \lambda_i \bar{C}_i, \end{cases} \quad (1)$$

where n is the neutron density; β_i , λ_i , are the characteristics of the i -th delayed neutron group; β is the fraction of delayed neutrons; ℓ^* is the prompt neutron lifetime; \bar{C}_i is the concentration of the i -th group delayed neutron precursors; ρ is the value of reactivity.

Ideally the output signal of simulator should correspond strictly to solution of differential equation system (1) with respect to $n(t)$ at constant value of reactivity which should be set in the simulator, i.e. output voltage $U(t)$ or current $I(t)$ versus time is given by:

$$I(t) = \frac{U(t)}{R} = \frac{U_0}{R} \sum_{i=1}^7 A_i e^{p_i t} = I_0 \sum_{i=1}^7 A_i e^{p_i t}, \quad (2)$$

where I_0 is the initial current at the simulator outlet; U_0 is the initial voltage at the simulator outlet; R is the resistance of current-forming resistor; p_i are the roots of characteristic equation resulted from (1); A_i are the coefficients whose values depend on the reactivity value set in the simulator.

In other words, ideally the output signal of the simulator should be formed such that the value calculated from this signal is identical to the set value. In reality this signal can have some deviations from the ideal one for a number of reasons. Consequently, there will be an error in the calculated reactivity value. For the sake of simplicity, this error is hereinafter referred to as the reactivity modeling error.

Until quite recently, a traditional approach to developing reactivity simulators has been to use analog simulation of reactor kinetics equations [4] where the connection between model and reactor parameters is determined by the following equations:

$$\lambda_i = \frac{1}{R_i C_i}; \quad \rho = \frac{R_{\parallel}}{R_{fb}}; \quad \frac{\ell^*}{\beta_i} = R_{\parallel} C_0;$$
$$\beta_1 R_1 = \beta_2 R_2 = \dots = \beta_6 R_6,$$

where ρ , β is the set value of reactivity; R_{\parallel} , Ω is the resistance equal to parallel connection of R_i ; R_{fb} , R_i , Ω are the corresponding values of resistance; C_i , C_0 , F are the corresponding values of capacitors.

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Figure 1 shows an electrical model of reactor kinetics, which corresponds to (2). The parameters of this model can be calculated using physical characteristics λ_i , ℓ^* and $\alpha_i = \beta_i / \beta$. A_1 is the measuring amplifie; A_2 , A_3 are the scaling amplifiers; C_0 is the capacity simulating prompt-neutrons lifetime; $R_i C_i$ are the six RC circuits, simulating six groups of delayed neutrons; VS is the voltage source for initial condition adjustment; R_{fb} is the set of feedback resistors, which determine the set reactivity; RT is the voltage-current resistive transducer; S_1 is the switch of voltage source; S_2 is the switch of modeling start; S_3 is the positive/negative reactivity switch.

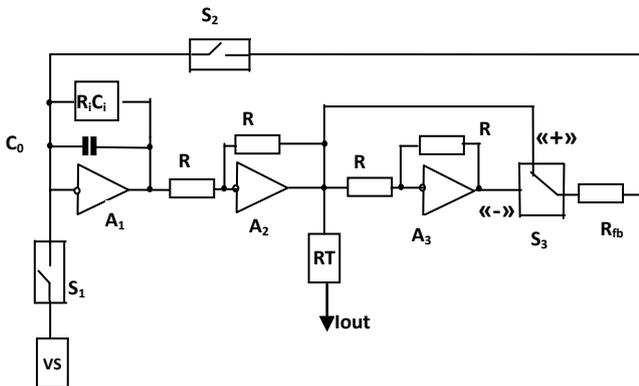


Figure 1. Electrical model of reactor kinetics (analog simulator of reactivity)

The main limitation of the analog circuit is slow changeover between simulation modes because long-time constants are needed for recovery of initial conditions in RC-circuits. In practice this leads to considerable time losses during preparation of the simulator for operation, because after each simulation change 5-10 minutes delay is required before the initial conditions can be set. Moreover, the parameters of RC-circuits of the analog simulator should be chosen taking into account a specific fuel composition or specific type of reactor. Therefore, modification of the electric circuit and its parameters is required to perform calibration of reactivity meters used for measurements in reactors with different fuel compositions or different type reactors. Finally, error of reactivity modeling sharply increases in analog simulators during formation of the output signal which corresponds to negative reactivity after a few decades of the output signal change («far-field error»), because in this case the desired signal value of the measuring amplifier decreases by a few decades and approaches becomes commensurable to the simulator noise.

2. Digital-to-Analog Simulator of Reactivity

A good alternative to analog simulator is a reactivity simulator based on digital-to-analog converter – the function which is widely used in different technical fields [5-7]. In D/A reactivity simulator output power signal is formed as output voltage of digital-to-analog converter (DAC), the law

of its time variation is set by a walking digital code which is formed either in real time from calculations or from values stored in memory.

The second alternative is preferable for a hardware implementation of the simulator because a minimum of hardware components are required: no microprocessor and only memory element and very simple circuits of data access control are needed.

A limiting factor for application of DAC-simulators is additional error due to discontinuity of DAC output voltage variation, while an error in the analog circuits is caused by the amplifier noise only. This additional error is especially strong during simulation of signals for negative reactivity with small absolute value. Figure 2 shows diagrams of relative error δ for modeling of reactivity with a set value of -0.1β using a simulator based on 12-bit DAC. As the diagram shows, this error sharply increases and becomes intolerable, $>1\%$, after half-decade of the power signal variation. In the same situation, a similar error for the analog simulator stays within 1% for power measurement within the whole decade.

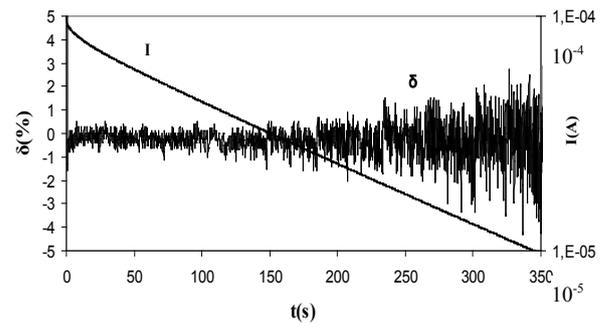


Figure 2. Processes in D/A reactivity simulator, which operates in direct control mode direct control of DAC by continuous power signal with one current-forming resistor connected and one decade of the power signal variation

In order to reduce this error the authors recommend the DAC-simulator [8] configuration given in figure 3. We use this diagram to illustrate the formation of a negative reactivity signal. In this configuration, the chosen interval of the power signal variation, which corresponds to the chosen reactivity, is preliminarily segmented and each of the segments corresponds to identical relative variation of this signal. For convenience, decadic segmentation is done.

Data array is entered in the memory storage. This data consists of N serial decades as a set of digital codes. Thus each of decades is prenormalized on the given number $A = 2^k$ by multiplication of the current values to value A/x_i , where k is a number of DAC bits, x_i is the value of power parameter at the beginning of i -th decade. Then a sequential sample of digital codes from the memory storage in program control unit is applied to the data-entry port P_{dac} .

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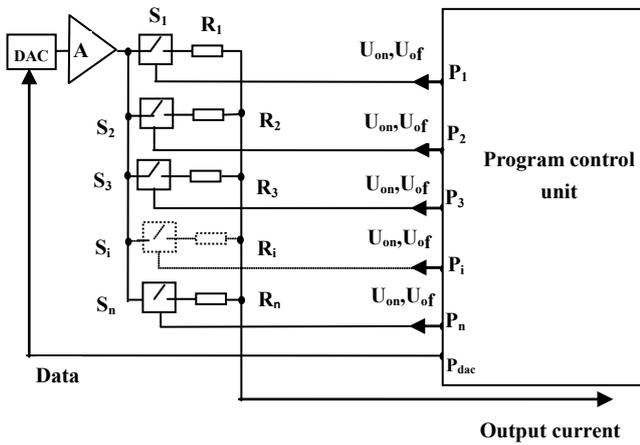


Figure 3. D/A simulator with decadic switching of power parameter. A is the measuring amplifier; S_i are electronic switches of current-forming resistors; R_i are the current-forming resistors; P_i are the ports for entry of keying signals; P_{dac} is the port of entry for control data of DAC

Such types of control data arrays can be formed for any specified value of reactivity; therefore the changeover between two different simulator modes, i.e. changeover between different initial current and different reactivity values during signal formation, takes almost no time. This changeover reduces itself to a selection of a control data array from the memory and connection of one of the electronic switches of current-forming set of resistors (selection of initial output current).

Figure 4 presents diagrams illustrating the simulator operation. It is shown that power parameter decades are normalized to the given value A (see vertical arrows in fig.4b) as the value of this parameter decreases (fig.4a) leading to a consequent change in the driving voltage level (fig.4c) and current forming resistance at $t_1, t_2, t_3, \dots, t_N$ in the end of decades (fig.4d). As a result, the simulator output current forms (fig. 4e), which corresponds to the change in the power parameter of the reactor which controls the reactivity value. Diagram 4c shows that in this simulator the signal-to noise ratio at the output port of the measuring amplifier has the same value in all decades of its output signal variation because the measuring amplifier output signal varies within only one decade in all decades of output signal variation of the simulator.

Another improvement of digital-to-analog applications for reactivity simulation problem is optimization of presentation of data stored in memory [9].

According to solution of the reactor kinetics equations, the reactor power for a fixed reactivity value begins to vary at an almost constant rate (one of the terms in the sum in the right-hand side of (2) becomes much greater than the others) at some moment after the reactivity jump.

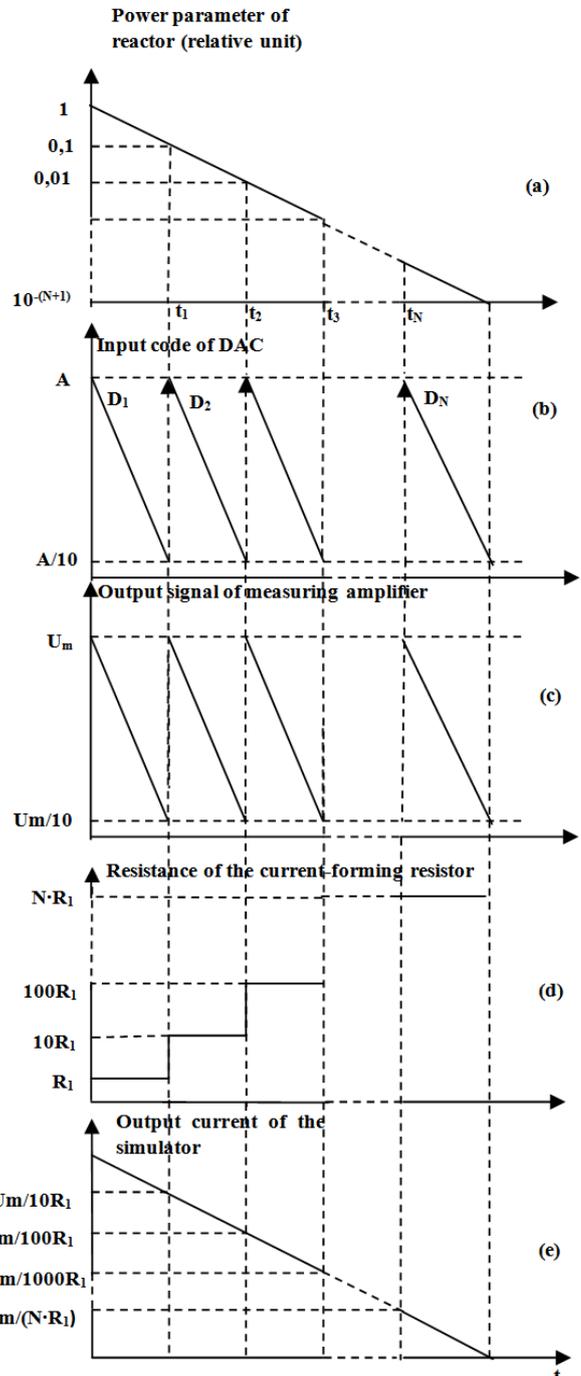


Figure 4. Processes in D/A reactivity simulator designed according to the diagram on the fig.3

Therefore, a signal variation within intervals (decades) can be duplicated beginning from a certain interval (decades) when segmenting the simulator output signal variation into intervals (decades). The interval suitable for beginning of duplication and possible number of duplicated intervals (decades) is determined by admissible error of reactivity value which the reactivity meter calculates from the modified signal. The error can be estimated from solution of

the reversed kinetics equation where reactor power is simulated by the modified signal. The performed calculations show that for practical reactivity values the error does not exceed 1% of the reactivity value, if the relative deviation of the simulated signal from the true one does not exceed 1% in each interval (decade) after the duplication.

Therefore, programming of the memory device in DAC-simulator does not require recording all the information for the selected time interval of the power signal variation. Only part of this information is quite sufficient and, thus, less memory volume is required. To illustrate, we now compare similar diagrams given in figure 4 and figure 5. Let us consider in detail the diagrams for standard-memory DAC-simulator and DAC-simulator with "reduced" memory volume. For both cases, in practice the normalizing number A was 4095 corresponding to the maximal capacity of the 12-bit DAC based simulator.

Obviously, for the standard-memory version, information about all decades of the power parameter variation should be stored in the simulator memory (see D_1, D_2, \dots, D_N in fig. 4b). A different behavior is observed for "reduced"-memory DAC-simulator. Diagrams in figure 5 show simulation of the power signal corresponding to reactivity value of -0.1β . The input code generation (fig. 5b) uses the first decade of the power parameter variation, normalized to A (fig. 5a) for interval between 0 and t_1 and the second decade of the power parameter variation, normalized to A for $t_1-t_2, t_2-t_3, \dots, t_N-T$ intervals, taking into account the second decade identity to all subsequent decades using constant ten-fold multiplier.

In this case it is sufficient to store information only about two decades of the power signal variation in the simulator memory as it is shown by D_1, D_2, \dots, D_2 (fig. 5b). The corresponding level variation of driving voltage (fig. 5c) and resistance of current-forming resistor at the end of decades (fig. 5d) is performed $K-1$ times during sampling of data corresponding to the end of the 1st decade (t_1 moment) and $N-K+1$ times during sampling of data corresponding to the end of the second decade (t_2, t_3, \dots, t_N moments), where N is the quantity of decades, K is the number of the decade where replacement of the actual signal by the duplicated one does not lead to a reactivity modeling error above 1%.

For $K=2$ six-decade power signal variation case, the mentioned level changes are performed one time ($K-1=2-1=1$) and during selection of data corresponding to the end of the first decade and five times ($N-K+1=6-4+1=5$) during the selection of data corresponding to the end of the second decade. As a result, the simulator output current is formed (fig. 5e), which adequately represents the initial power parameter change for reactivity control using as little data as possible needed for the reactor power signal simulation.

Since the reactivity simulator should provide a set of reactivity values characterizing for a task to perform (calibration or functional check of the reactivity meter), then each reactivity value corresponds to a specific K value, as it was mentioned before. Therefore, the reduction of the storage memory volume of the simulator as a whole is

slightly lower than a similar reduction of data array calculated for one value of reactivity with a small absolute magnitude ($\pm 0.1\beta$). As an example, for a practical set of reactivity values the above mentioned optimization of data provides 26 % and more than two-fold reduction of the memory volume for continuous simulation of reactivity in three and six decades of the power signal variation, respectively (see Table 1 and 2).

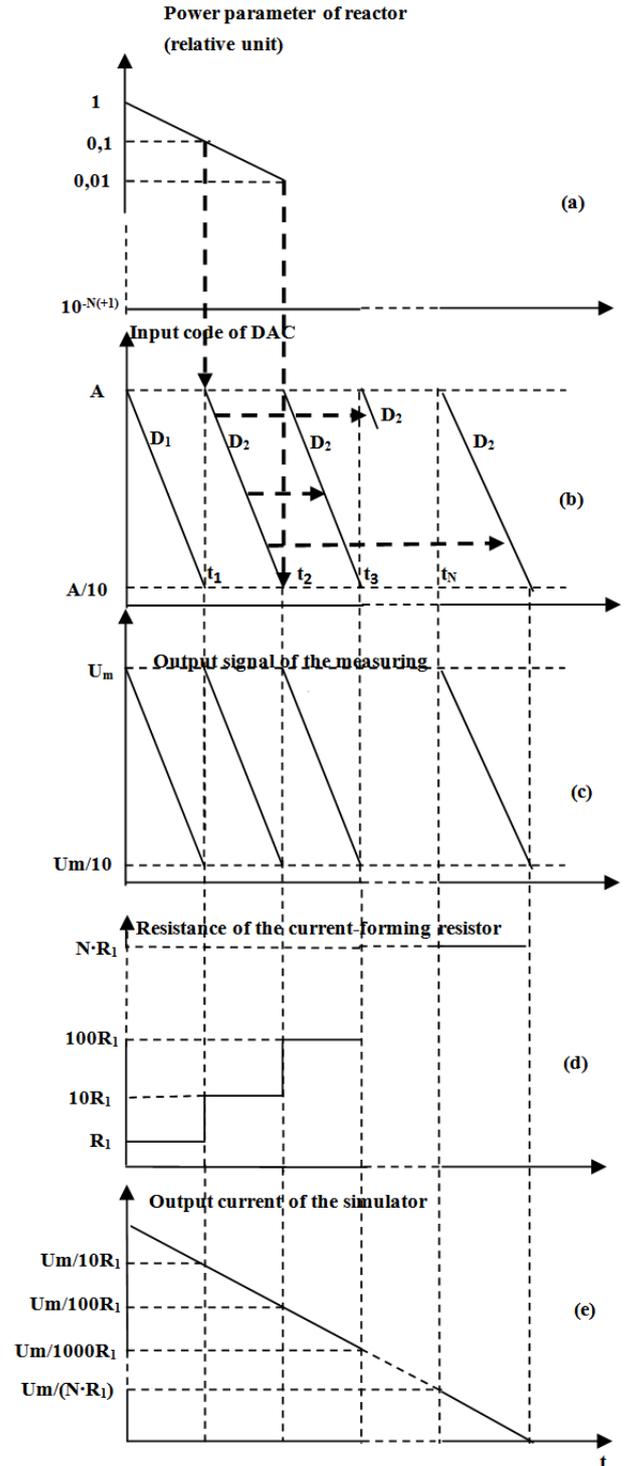


Figure 5. Processes in D/A reactivity simulator with «reduced» memory storage

3. Experiments

Figure 6 shows the time variation of the power signal and corresponding error of reactivity $\rho = -0.1\beta$ modeled by the simulator shown in fig. 3. The simulation was performed in three decades of the power signal variation using the “reduced” memory 12-bit DAC based simulator. Let us note that the purpose of the current study was to obtain the value of error for reduce-memory DAC simulator as good as the value of error for analog simulator ($\approx 1\%$). This problem has successfully been solved. It may be assumed that standard-memory DAC simulator would have much less error, but this fact wasn’t proved experimentally.

Figure 7 shows similar diagrams for the case with direct control of DAC by continuous power signal with one current-forming resistor connected. The comparison between fig. 7 and fig. 6 illustrates advantages of the proposed methods as applied to DVA reactivity simulators.

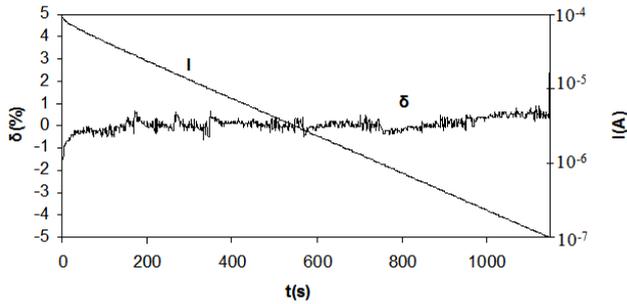


Figure 6. Time history of current I and relative error δ of reactivity simulation $\rho = -0.1\beta$ for DVA reactivity simulator with «reduced» memory storage

In particular, the diagram in figure 6 shows that the error of reactivity simulation exceeds 300% at the end of the third decade of the power signal variation. We also can see that this error exceeds $\pm 1\%$ even at the first half-decade as mentioned above. Based on this, it can be concluded that staying in the error range of $\pm 1\%$ using 12-bit DAC requires formation of the power signal by “sewing” of power signal variation half-decades with appropriate switching between current-forming resistors. Data given in fig. 6 is obtained from «sewing» of six half-decades.

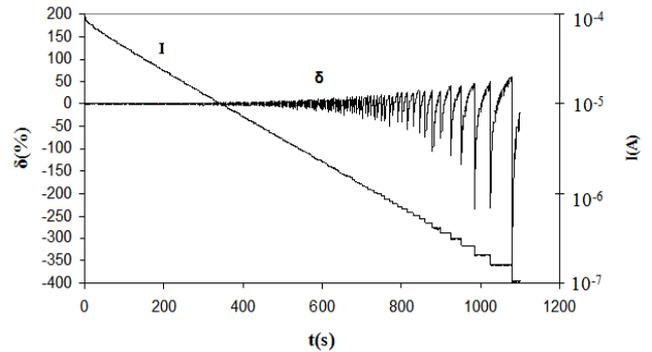


Figure 7. Time history of current and relative error for simulation of $\rho = -0.1\beta$ reactivity of direct control of DAC by continuous power signal with one current-forming resistor connected

Table 3 shows the current values of control codes for 12-bit DAC at selected points of half-decade «sewing» and corresponding values of current-forming resistor resistances and output currents.

Table 1. Comparison of standard and reduced memory volumes for three decades of power variation

ρ, β	Number of decades, where the discrepancy of the reactivity calculated for normalized decades does not exceed 1%	Volume of data array for three decades (number of words in memory)	Volume of data array for normalized decades (number of words in memory)
-0,04	2	24721	16338
-0,1	2	11321	7360
-0,2	3	6952	6952
-0,5	5	4323	4323
-1	5	3274	3274
-2	5	2534	2534
-5	> 6	1799	1799
-10	> 6	1367	1367
+0,04	2	19840	13124
+0,1	2	6562	4293
+0,2	2	2377	1528
+0,5	3	341	341
		Total volume of data array for three decades	Total volume of data array for normalized decades
		(number of words in memory)	(number of words in memory)
		Relative unit	Relative unit
		85411	63233
		1	0,74

Table 2. Comparison of standard and reduced memory volumes for six decades of power variation

ρ, β	Number of decades, where the discrepancy of the reactivity calculated for normalized decades does not exceed 1%	Volume of data array for six decades (number of words in memory)	Volume of data array for normalized decades (number of words in memory)
-0,04	2	49850	16338
-0,1	2	23211	7360
-0,2	3	14782	6952
-0,5	5	10418	8382
-1	5	9020	7092
-2	5	8121	6230
-5	> 6	7200	7200
-10	> 6	6582	6582
+0,04	2	39986	13124
+0,1	2	13400	4293
+0,2	2	4923	1528
+0,5	3	736	341
		Total volume of data array for six decades	Total volume of data array for normalized decades
		(number of words in memory)	(number of words in memory)
		Relative unit	Relative unit
		188229	85422
		1	0,45

Table 3. Decadic sewing of 12-bit DAC

Task code	Resistance of the current-forming resistor*[M Ω]	Output current [A]	DAC reference voltage of the measuring amplifier [V]	Decade number
4095	0,05	$0,1006 \cdot 10^{-3}$	5,0	1
1147		$0,2816 \cdot 10^{-3}$	1,4	
4095	0,1785	$0,2814 \cdot 10^{-3}$	5,0	
1454		$0,0997 \cdot 10^{-4}$	1,77	
4095	0,5	$0,0998 \cdot 10^{-4}$	5,0	2
1147		$0,2806 \cdot 10^{-5}$	1,4	
4095	1,785	$0,2796 \cdot 10^{-5}$	5,0	
1464		$0,0999 \cdot 10^{-5}$	1,78	
4095	5	$0,0996 \cdot 10^{-5}$	5,0	3
1147		$0,2783 \cdot 10^{-6}$	1,4	
4095	17,85	$0,2783 \cdot 10^{-6}$	5,0	
1464		$0,0998 \cdot 10^{-6}$	1,78	

4. Conclusions

Testing of the described methods for designing D/A simulators of reactor kinetics and also methods for grouping and presentation of control data showed their advantages over traditional analog simulators. The D/A simulators are ready to use immediately after a change between operation modes and have almost invariable level of the relative deviation from its specified value in reactivity corresponding to DAC-simulator output signal. The deviation is within at least three decades of the power signal variation. Use of the obtained data in designing D/A simulators can significantly improve their performance characteristics.

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