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Fabrication and Analysis of Carbon Doped Hydrogenated Amorphous Silicon Thin Film Transistors

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Abstract Thin film transistors (TFT) are mainly used in display devices such as a LCD display or a LED display, as a current switch. This paper focuses on analysis of thin film transistors fabricated using carbon doped amorphous silicon as the semiconductor layer (a-Si:C:H). Radio Frequency Plasma Enhanced Chemical Vapour Deposition (RF-PECVD) technique was used to deposit the semiconductor active layer of a-Si:C: H as well as the dielectric silicon nitride layer. Thermal evaporation was used for depositing Aluminium as the gate, source and drain electrodes. Results from UV-VIS-NIR spectrophotometer suggests that the optimised semiconductor active layer with a thickness of 113 nm, exhibited a bandgap value of 1.88 eV. The TFT based on this a-Si:C:H showed linear I-V characteristics as measured using a semiconductor device analyser. Further a thin layer of diborone (B_2H_6) doped p type a-Si: H was added on top of the active layer (a-Si:C:H) and the TFT thus built showed diode characteristics at the Aluminium- p doped a-Si: H interface. It was thus learnt that using n–doped semiconductor layer with aluminium as the contact electrode provides better TFT characteristics than using Aluminium directly as the source drain material.

Keywords a-SiC:H, RF-PECVD, Tauc Plot, TFT

1. Introduction

Thin film transistors (TFT) form a very important component in the displays such as LCDs and LEDs, where they are mainly used as switching elements that drive the current to the pixels. With the growing demand for flat panel displays, extensive research has been carried out in this field to find the optimum semiconductor active layer material, which can drive large currents, when incorporated in a TFT. As pointed out in [2], extensive research has been carried out on compound materials such as CdSe, to test their applicability in TFTs. However, they have not been introduced into the industry. Among all such materials researched, hydrogenated amorphous silicon (a-Si:H) was chosen as the semiconductor layer, which could be deposited using a Plasma Enhanced Chemical Vapour Deposition technique (PECVD) and has lesser process steps, making it easier to produce on large scale. However, a-Si:H TFTs have low charge mobilities (>1 cm^2/Vs) [2]. Hence they can be used to drive current only to LCD pixels functioning at low frequencies and not OLEDs which generally need a larger drive current. This requirement prompted further research into TFTs and alternative materials such as poly-Si and organic semiconductors have been tested for the same. In poly-Si TFTs, the number of stages required to create poly-Si structures are more and alternative methods such as metal-induced crystallization and pulsed rapid thermal annealing have been used but they don't possess uniform grain sizes. On the other hand, organic semiconductor thin films could be easily deposited using vacuum less technologies such as spin coating and hence can be looked up as cheaper alternatives for the conventional vacuum oriented thin film coatings. But these materials need very high gate driving voltages and are also unstable in air.

A material such as SiC was also tested as the semiconductor material in TFTs in [1]. Accordingly, an amorphous layer of hydrogenated SiC (a-SiC: H) was first coated and then crystallized using KrF UV excimer laser annealing. The bandgap obtained for this material coating was between 1.9 -2.1 eV [1]. Use of SiC in a TFT has breakdown voltages as high as $2.4x10^6$ V/cm [4] and hence it will work efficiently even at very high applied electric fields. However the larger bandgap values of SiC will make the switching happen at relatively larger gate voltages.

Considering all the above factors, TFTs made up of a-Si: H doped with small amounts of carbon were tested as the semiconductor material and its analysis is provided in this paper.

The organization of the paper is as follows:

1. Introduction
2. Chemical composition and material analysis of SiC
3. Structure of the Thin film transistor

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4. TFT Gate, Source and Drain material- Aluminium
5. TFT dielectric material-Silicon Nitride
6. TFT semiconductor material- a-Si:C:H
7. Material Characterization
8. Results
9. Conclusion and future scope

2. Experimental

a. Chemical composition and material analysis of a- Si:C:H

PECVD was used to deposit a-Si:C: H layers, using Silane (SiH_4), Methane (CH_3) and Hydrogen (H_2) as the precursor gases. Accordingly, the ratio of the gases used determines the composition of the coated material [3]. This is further substantiated in the parameter 'Y' equation [3].

$$Y = V_{CH4} / (V_{CH4} + V_{SiH4}) \quad (1)$$

Where V_{CH4} and V_{SiH4} represent volumes of Methane and Silane respectively in standard cubic centimetres (sccm) and the ratio Y is used as a parameter to determine the chemical composition of the coating [3]. The value of Y can range between 0 to 1, which indicates that as the value of 'Y' increases, the amount of carbon doping also increases.

b. Structure of the thin film transistor:

Owing to the better transistor characteristics obtained in a bottom gate structure, as compared to a top gate structure, the former has been used as the TFT structure. The TFTs thus built have the following structure:

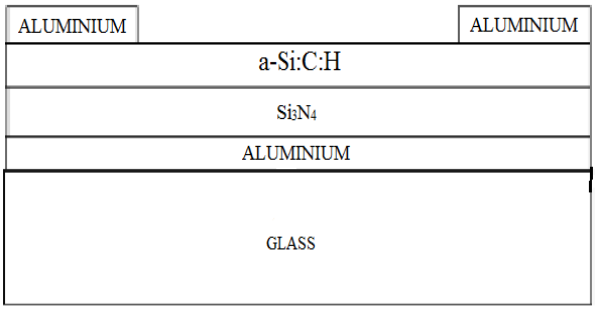

Figure 1. Bottom gate TFT structure

TFTs were built using stainless steel shadow masks, which used laser etching to obtain microscale dimensions of required length and width respectively. These were mainly designed for a long channel length of 100 µm and the width of the transistor chosen was 150 µm.

c. TFT gate, source and drain material - Aluminium:

With the use of shadow masks, which use bottom up approach for coating, both magnetron sputtering and thermal evaporation techniques were studied in detail for depositing the electrodes (gate, source and drain). It has been understood in the case of sputtering that the dimensions of the deposited gate electrode were compromised due to the smaller dimensions of the masks leading to narrowing down and discontinuous channel widths; whereas the gap between the source and drain was reduced as well as short circuited because of the higher penetrating energies of the sputtered atoms. Hence thermal evaporation is preferred to deposit the electrodes even though sputtered electrodes showed lower contact resistance.

To improve the adhesion of Aluminium gate electrode on the glass substrate, after subjecting the substrate to the standard chemical cleaning and drying procedures, the substrate surface was oxygen plasma treated using Ion Bombardment (IB) technique and the process parameters for the same are: Initial vacuum - $1x10^{-5}$ mbar, working pressure- $5x10^{-2}$ mbar, time – 18 min. After treatment, Aluminium pellets were evaporated in a hot filament at a controlled evaporation rate of 100 A^o/s to get the required thickness of 300 nm. As aluminium is used as both contact electrode and the source/drain region, a thickness of 300nm was chosen to detect any small change in current through the transistor.

d. TFT gate dielectric material- Silicon Nitride

Radio frequency Plasma Enhanced Chemical Vapour Deposition (RF-PECVD) technique is used to deposit Si3N4 and a-SiC: H thin films. The system consists of 5 individual process chambers supported by magnetic arms and a central transfer chamber. The operation and control of the machine as well as the process are done through SCADA software. A base vacuum of around 10^{-6} mbar is created using rotary-roots-turbo pumps combination, prior to each deposition, while the process pressure of 0.5-1.0 Torr is maintained through a dry pump.

Silicon Nitride (Si_3N_4) is a popular dielectric material used in the semiconductor industry, owing to its superior insulator properties and passivation properties. However, when it is coated on large panel displays, the deposition conditions will determine the tensile stress and the compressive stress [5]. If the tensile stress is very high, the Si_3N_4 coating will cut off in between while a large compressive stress will result in Si_3N_4 material peel off.

Considerable efforts were made to study the process parameters in order to obtain good quality Si_3N_4 films with reduced stress. The optimised process parameters are: RF power-10W, Operating pressure-0.5 Torr, substrate temperature- 250°C, Ammonia (NH_3) gas inflow- 100 sccm, Silane (SiH_4) gas inflow- 10 sccm. The deposition rate has been maintained around 12nm/min.

e. TFT semiconductor material- a-Si:C:H:

As mentioned in equation (1), the ratio of precursor gases namely Methane, Silane and Hydrogen determine the composition of the active layer. Hence when Y=0.1, a-SiC: H coating mainly contains Si-Si bonds and nearly no Si-C bonds while when Y=0.2, the bonds are again predominantly Si-Si with a small number of Si-C bonds. Therefore as the value of Y increases, the number of Si-C bonds also increases. For example in [6], for a chamber temperature of 300°C, the value of parameter Y is 0.95 which implies that the pre-dominant bonding in these coatings is Si-C. In this paper, the value of Y considered is 0.2. By theory, these are

predominantly, Si-Si bonded atoms, with small amounts of Si-C bonds. The PECVD process parameters employed for depositing a-Si:C:H layer are: Temperature=250°C, Respective inlet gases composition in sccm: H_2=100, CH_4=2, SiH_4=10, Operating pressure = 1Torr, RF power = 7W and the rate of deposition was 2.5 nm/min.

An extra thin layer of B_2H_6 doped p doped a-Si:H was added on top of a-Si:C:H semiconductor layer in one of the samples, using PECVD and the I-V characteristics of this TFT was compared with the a-Si:C:H TFT samples without a p-doped a-Si:H layer. This thin film was deposited using PECVD and the process parameters for this thin film are: RF power = 7W, Time = 4 min, Respective inlet gases composition in sccm: B_2H_6=6, CH_4=8, SiH_4=10, H_2=100, Temperature= 250°C, Operating pressure = 1 Torr.

f. Materials Characterization:

The thickness of each of the coatings was carried out using stylus profilometer. To obtain the material band gap, UV-Vis-NIR spectrophotometer was utilized. The calculation of the band gap was done using the TAUC equation (2) [7].

$$\alpha h\upsilon = A(h\upsilon - E_g)^n \quad (2)$$

Where h is Planck's constant, υ is the frequency of incident radiation, E_g is the optical band gap of the material, α is co-efficient of absorption and A is a constant. Being an indirect transition, the value of n will be 2. Using a Tauc plot, we can obtain the optical band gap of the material under observation. However, if the material is amorphous in nature, its optical band gap can be approximated to the bandgap between its valence and conduction band.

To confirm the presence and the amorphous nature of the coated material (a-SiC: H), Raman spectroscopy was utilized. Atomic Force Microscopy (AFM) was also utilized to obtain this material's surface topology. The device thus built was electrically characterized using B1500A semiconductor device analyser.

3. Results

The thickness of the optimised aluminium electrodes was around 300 nm thick with a contact resistance of 0.8 Ω. Similarly the Si3N4 thin films had a thickness of 400 nm and exhibited a band gap of 2.81 eV with a contact resistance of 2.94 GΩ. The a-Si:C:H semiconductor active layer has been optimized for a layer thickness of around 113 nm and a bandgap of 1.88 eV. Raman spectroscopy was carried out on the active layer samples to confirm the presence of Si-C bonding of a-Si:C:H. Fig. 2 shows the recorded Raman spectrum of the active layer which confirms the amorphous nature of the films and the peak obtained at 494 cm^{-1}, confirms the presence of a-Si:C:H which clearly indicates the Raman shift from that of the pure a-Si:H at 481 cm^{-1} wave number.

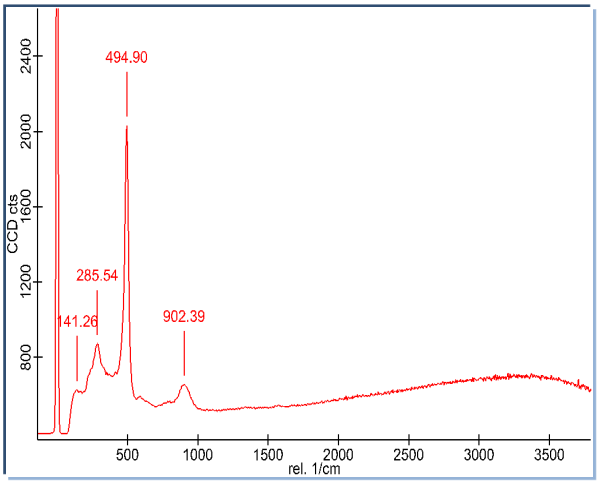

Figure 2. Raman spectrum of a-Si:C:H

Fig. 3 shows the surface morphology of the active layer characterized through AFM.

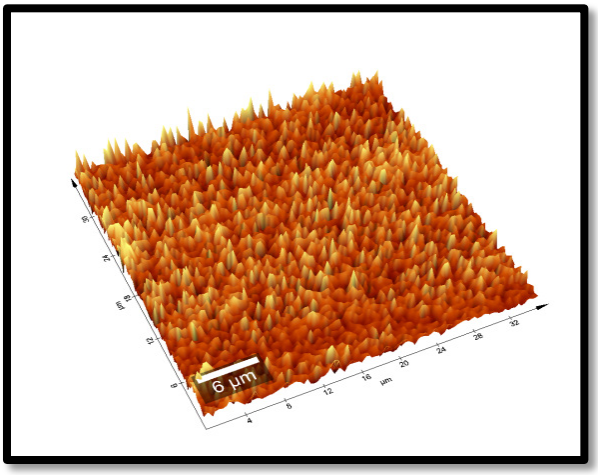

Figure 3. Surface topology of a-Si:C:H as seen by an AFM

Fig. 4 and Fig. 5 shows the optical spectrum and the calculated tauc plot of the a-SiC: H active layer. As the material considered here, a-SiC: H is amorphous in nature, the Tauc plots obtained in Fig. 5 were utilized to calculate their band gap using equation (2). The band gap values obtained for the same was 1.88 eV.

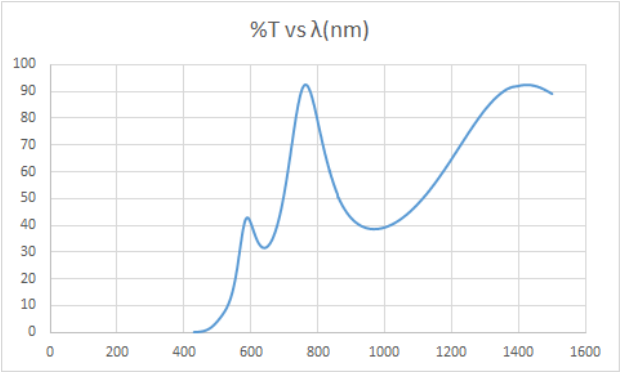

Figure 4. Transmission curve for a-Si:C:H thin film

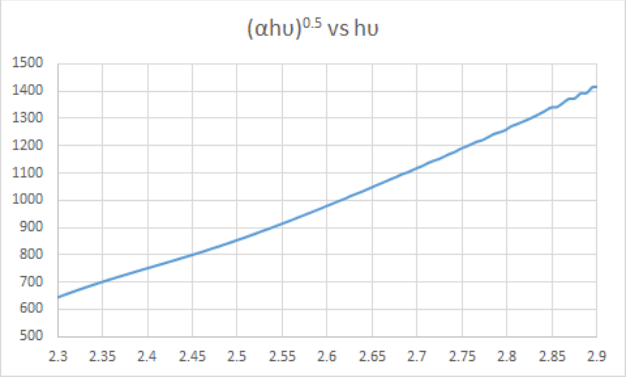

Figure 5. Tauc plot for calculating bandgap of a-SiC: H

Agilent device analyser B1500A was used to obtain the I-V characteristics of a-SiC: H TFT. Fig. 6 and Fig. 7 show the Id vs Vds characteristics of a-Si:C:H TFT and a-Si:C: H TFT with an extra p layer on the active layer respectively.

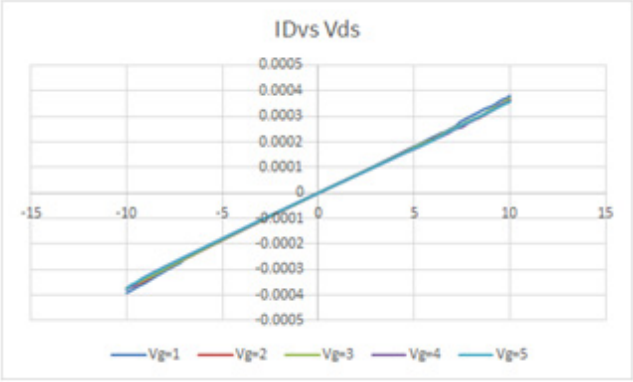

Figure 6. Id vs Vds characteristics of a-Si:C: H TFT without an extra added layer of boron doped a-Si

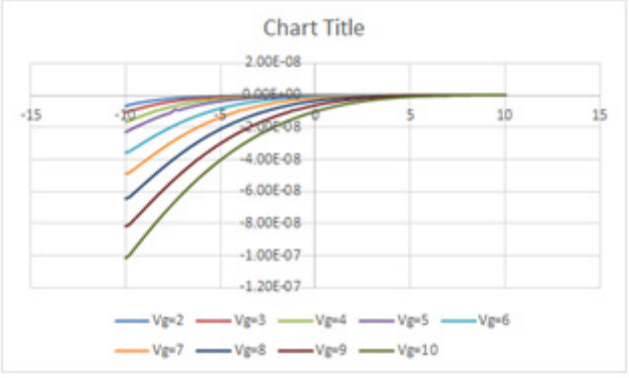

Figure 7. Id vs Vds characteristics of a-Si:C:H TFT with a small added layer of boron doped a-Si

4. Conclusions and Future Scope

a-Si:C: H is corrosion resistant, has relatively large band gap and also has good stability at high frequencies. Hence owing to its semiconductor nature, TFTs based on them were fabricated and analysed for a particular precursor gas ratio of SiH_4, CH_4 and H_2. The presence of a-Si:C: H as an active layer was confirmed by Raman spectroscopy.

The TFTs were fabricated on a glass substrate with bottom gate configuration. Oxygen plasma treatment was used to achieve good adhesion of the gate material aluminium on to the substrate. The electrical contact resistance of the obtained aluminium thin film was found to be 0.8 Ω. Suitable thickness of a-Si:C: H and Si_3N_4 dielectric were chosen and they were accordingly coated on the Gate material aluminium. Aluminium was again coated on top of these materials as the source and drain regions. In addition, TFTs were prepared by adding a thin layer of boron doped a-Si in between the semiconductor active layer and the source-drain regions.

The band gap of the same material was calculated using a Tauc plot obtained from its transmission characteristics. The I-V characteristics of the two different TFTs were compared and it was found that:

1. With the lack of major charge carriers such as the holes and electrons, aluminium and a-SiC: H junction acts like a resistor with very high resistance and hence we obtain a linear graph as shown in Fig.6. The large thickness of Aluminium, helps in detecting any small change in current that passes through the transistor.
2. It may be learnt from the experiment that the lack of depletion region in the Al- a-Si:C: H junction is due to the lower value of 'Y' selected for the PECVD growth of a-Si:C:H thin film.
3. Upon addition of a thin layer of boron doped a-Si on the a-SiC thin film, the current 'Ids' increased with increasing gate voltage but the junction of aluminium and boron doped a-Si layer now shows diode characteristics (schottky contact) as shown in Fig.7. Boron doping, unlike in the previous step provides charge carriers but due to the schottky contact developed with the aluminium layer, all current that flows through is contact has an inherent rectifying action associated with it.
4. To obtain good TFT characteristics, the source and drain regions could be a doped semiconductor thin film and aluminium can be used as their contact electrodes, instead of using aluminium directly as the source and drain regions.

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